

MLCAD Program 2024

Sunday, Sept. 8, 2024	
18:30-21:00	Welcome Reception
Monday, Sept. 9, 2024	
07:30-08:30	Breakfast
08:30-08:45	Opening Remarks
08:45-09:30	Keynote 1: Jeffrey David, VP of AI Solutions at PDF Solutions Advancing AI Innovations at Scale for Semiconductor Manufacturing and Test Moderator: <i>Hussam Amrouch - Technical University of Munich</i>
09:30-09:45	Break
09:45-10:45	Session 1: High-Level Synthesis Moderator: <i>Cong Callie Hao - Georgia Institute of Technology</i> Learning to Compare Hardware Designs for High-Level Synthesis <i>Yunsheng Bai, Atefeh Sohrabizadeh, Zijian Ding, Rongjian Liang, Weikai Li, Ding Wang, Haoxing Ren, Yizhou Sun, Jason Cong</i> Cross-Modality Program Representation Learning for Electronic Design Automation with High-Level Synthesis <i>Zongyue Qin, Yunsheng Bai, Atefeh Sohrabizadeh, Zijian Ding, Ziniu Hu, Yizhou Sun, Jason Cong</i> Automated C/C++ Program Repair for High-Level Synthesis via Large Language Models <i>Kangwei Xu, Grace Li Zhang, Xunzhao Yin, Cheng Zhuo, Ulf Schlichtmann, Bing Li</i> An ML-aided Approach to Automatically Generate Schematic Symbols in PCB EDA Tools <i>Shiyu Gao, Keni Qiu</i>
10:45-11:15	Break

<p>11:15-12:00</p>	<p>Session 2: Logic Synthesis Moderator: <i>Cunxi Yu, University of Maryland</i></p> <p>ReLS: Retrieval Is Efficient Knowledge Transfer For Logic Synthesis <i>Rongjian Liang, Chia-Tung Ho, Anthony Agnesina, Wen-Hao Liu, Haoxing Ren</i></p> <p>Efficient Subgraph Matching Framework for Fast Subcircuit Identification <i>Bohao Li, Shizhang Wang, Tinghuan Chen, Qi Sun, Cheng Zhuo</i></p> <p>MinBLoG: Minimization of Boolean Logic Functions using Graph Attention Network (BPA Nominee) <i>Prianka Sengupta, Vivek K Rajan, Hesham Mostafa, Somdeb Majumdar, Aakash Tyagi, Jiang Hu</i></p>
<p>12:00-13:00</p>	<p>Lunch</p>
<p>13:00-14:15</p>	<p>Special Session 1 (Invited) Moderator: <i>Jiang Hu, Texas A&M University</i></p> <p>A3C3 – AI Algorithm & Accelerator Co-design, Co-search, and Co-generation <i>Deming Chen, UIUC</i></p> <p>Automating Data Specialization for Machine Learning Acceleration <i>Zhiru Zhang, Cornell</i></p> <p>Machine Learning for High Sigma Analog Designs <i>Srinivas Jallepalli, NXP Semiconductor</i></p>
<p>14:15-14:45</p>	<p>Break</p>

14:45-15:30	<p>Session 3: Timing Modeling and Analysis Moderator: <i>Yibo Lin, Peking University</i></p> <p>FACT: Fast and Accurate Multi-Corner Predictor for Timing Closure in Commercial EDA Flows <i>Jiajie Xu, Ziyue Han, Leilei Jin, Shiyang Wu, Hao Yan, LongXing Shi</i></p> <p>Cell Library Characterization for Composite Current Source Models Based on Gaussian Process Regression and Active Learning <i>Tao Bai, Zeyuan Deng, Peng Cao</i></p> <p>ML-TIME: ML-driven Timing Analysis of Integrated Circuits in the Presence of Process Variations and Aging Effects <i>Xuanyi Tan, Peter Domanski, Sanmitra Banerjee, Krishnendu Chakrabarty</i></p>
15:30-16:00	<p>Break & Interactive Session 1</p> <p>FAMOUS: Flexible Accelerator for Attention Mechanism of Transformer on UltraScale+ FPGAs <i>Ehsan Kabir, Md Arafat Kabir, Austin R.J. Downey, Jason Bakos, David Andrews, Miaoqing Huang</i></p> <p>Predicting FPGA Routing Time with ML <i>Andrew David Gunter, Steven J E Wilton</i></p> <p>LASGNA: Large-scale Analog Surrogate Modeling for General Neuromorphic Architectures <i>Jason Ho, James Andrew Boyle, Andreas Gerstlauer</i></p>
16:00-17:30	<p>Tutorial 1: Accelerating Semiconductor Industry Innovation with AI/ML: Materials Discovery, Process Optimization, Device Engineering, Chip Design</p> <p><i>Speakers: Gaurav Thareja, Shruba Gangopadhyay, Sravan Nandakumar, Federico Nardi, Sriram Madhavan - Applied Materials</i></p> <p><i>Moderator: Hussam Amrouch, TUM</i></p>
17:30-18:00	<p>Break & Refreshing</p>
18:00-19:30	<p>Dinner and Networking</p>
19:30-21:00	<p>Panel: ML Enabled CAD – Buy or Develop In-House? Organizer: <i>Paul Franzon</i></p> <p>Panelists:</p>

	<p><i>Matt Hogan, Siemens</i> <i>Mark Ren, NVIDIA</i> <i>Thomas Andersen, Synopsys</i> <i>Lorenzo Servadei, Sony</i> <i>Rajeev Jain, Qualcomm</i></p>
Tuesday, Sept. 10, 2024	
07:30-08:30	Breakfast
08:30-09:15	Keynote 2: <i>Jinjun Xiong, University at Buffalo</i>
09:15-09:30	Break
09:30-10:30	<p>Session 4: Physical Design I Moderator: <i>Vidya Chhabria - Arizona State University</i></p> <p>Optimizing Predictive AI in Physical Design Flows with Mini Pixel Batch Gradient Descent <i>Haoyu Yang, Anthony Agnesina, Haoxing Ren</i></p> <p>Enabling Risk Management of Machine Learning Predictions for FPGA Routability <i>Andrew David Gunter, Maya Thomas, Nikhil Pratap Ghanathe, Steven J E Wilton</i></p> <p>Machine Learning VLSI CAD Experiments Should Consider Atomic Data Groups <i>Andrew David Gunter, Steven J E Wilton</i></p> <p>OpenROAD-Assistant: An Open-Source Large Language Model for Physical Design Tasks <i>Utsav Sharma, Bing-Yue Wu, Sai Rahul Dhanvi Kankipati, Vidya Chhabria, Austin Rovinski</i></p>
10:30-11:00	<p>Break & Interactive Session 2</p> <p>FlexCELL: Flexible Standard Cell Design with Heterogeneous Graph Neural Network <i>Jakang Lee, Jongho Yoon, Junseok Hur, Sehyeon kim, Sunmean kim, Seokhyeong Kang</i></p>

	<p>Interactive and Automatic Generation of Primitive Custom Circuit Layout Using LLMs <i>Geunyoung You, Youjin Byun, Sojin Lim, Jaeduk Han</i></p> <p>MAPP: Machine Learning Assisted Placement Predictions for Improving Standard Cell Synthesis <i>Luke Thomas, Sriram Madhavan, Andres Llopis, Ivo van Zandvoort, Maarten Berkens</i></p> <p>Sensitivity Analysis for Active Sampling, with Applications to the Simulation of Analog Circuits <i>Reda Chhaibi, Fabrice Gamboa, Vinicius Oliveira, Christophe Oger, Clément Pellegrini, Damien Remot</i></p>
<p>11:00-11:45</p>	<p>Session 5: Physical Design II Moderator: <i>Jiaqi Gu, Arizona State University</i></p> <p>TA3D: Timing-Aware 3D IC Partitioning and Placement by Optimizing the Critical Path <i>Donggyu Kim, Minjae Kim, Junseok Hur, Jakang Lee, Jinoh Cho, Seokhyeong Kang</i></p> <p>Flip-flop Centric Incremental Placement for Simultaneous Timing and Clock Network Power Optimization <i>Cristhian Roman-Vicharra, Yiran Chen, Jiang Hu</i></p> <p>Human Language to Analog Layout Using Glayout Layout Automation Framework <i>Ali Hammoud, Chetanya Goyal, Sakib Pathen, Arlene Dai, Anhang Li, Gregory Kielian, Mehdi Saligane</i></p>
<p>12:00-13:00</p>	<p>Lunch</p>
<p>13:00-14:30</p>	<p>Special Session 2 (Invited) Moderator: <i>Youngsoo Shin - KAIST</i></p> <p>Redefining Outliers in Wafer-Based Electrical Testing <i>Takashi Sato, Kyoto University</i></p> <p>LLM-Assisted Analytics in Semiconductor Test <i>Li-C Wang, UCSB</i></p> <p>Machine Learning in Logic Circuit Diagnosis <i>Shawn Blanton, CMU</i></p>

	<p>When Device Modeling Meets Machine Learning: Opportunities and Challenges <i>Lining Zhang, Peking University</i></p>
14:30-14:45	Break
14:45-15:30	<p>Session 6: Datasets and Benchmarks Moderator: <i>Ulf Schlichtmann, Technical University of Munich</i></p> <p>AutoBench: Automatic Testbench Generation and Evaluation Using LLMs for HDL Design <i>Ruidi Qiu, Grace Li Zhang, Rolf Drechsler, Ulf Schlichtmann, Bing Li</i></p> <p>HLSFactory: A Framework Empowering High-Level Synthesis Datasets for Machine Learning and Beyond (BPA Nominee) <i>Stefan Abi-Karam, Rishov Sarkar, Allison Seigler, Sean Lowe, Zhigang Wei, Hanqiu Chen, Nanditha Rao, Lizy Kurian John, Aman Arora, Callie Hao</i></p> <p>Thermal Map Dataset for Commercial Multi/Many Core CPU/GPU/TPU <i>Jincong Lu, Sheldon Tan</i></p>
15:30-16:00	<p>Break & Interactive Session 3</p> <p>VLSI Hypergraph Partitioning with Deep Learning <i>Muhammad Hadir Khan, Bugra Onal, Eren Dogan, Matthew Guthaus</i></p> <p>Large Reasoning Models for 3D Floorplanning in EDA: Learning from Imperfections <i>Shafin Amin, Nirjhor Rouf, Tse-Han Pan, Md Kamal Ibn Shafi, Paul Franzon</i></p> <p>Smart Multipatterning in EDA: An RL-GNN Approach to Constrained Graph Coloring <i>Abdelrahman Wael Mohamed Helaly, Nourhan Sakr</i></p>
16:00-17:30	<p>Student Hands-on Workshop by Synopsys</p> <p>Organizer: <i>Stelios Diamantidis</i> Presenter: <i>Dr. Sean Safarpour</i></p> <p>Title: <i>Lowering the Bar for Formal Verification Adoption with VC Formal and Generative AI</i></p>
17:30-19:00	Outside Activities in the Beautiful Snowbird Mountains
19:00-20:30	Dinner

Wednesday, Sept. 11, 2024

07:30-08:30

Breakfast

08:30-09:15

Keynote 3: Michael Spranger, COO of Sony AI Inc.
Next-Generation AI for Image Sensing and Entertainment

Moderator: *Andrew Kahng, UC San Diego*

09:15-09:45

Break

09:45-10:30

Session 7: Power Grid Analysis and Optimization

Moderator: *Lining Zhang, Peking University*

ICDaIR: Distribution-aware Static IR Drop Prediction Flow Based on Image Classification

Pinquan Li, Yunfan Zuo, Yuwei Sun, Hao Yan, Longxing Shi

IR-Aware ECO Timing Optimization Using Reinforcement Learning (BPA Nominee)

Wenjing Jiang, Vidya Chhabria, Sachin Sapatnekar

A Parallel Simulation Framework Incorporating Machine Learning-Based Hotspot Detection for Accelerated Power Grid Analysis

Yangfan Jiang, Jianfei Song, Xiaoyu Yang, Xiao Dong, Songyu Sun, Yibo Lin, Zhou Jin, Xunzhao Yin, Cheng Zhuo

10:30-11:00

Break & Interactive Session 4

Evaluation of Open-Source Large-Language-Models for Verilog Code Generation

Daniel Kiesewalter, Andrea Bonetti, Francesco di Stefano, Eisaku Ohbuchi, Malte J. Rasch, Lorenzo Servadei

Boosting Productivity of Hardware Documentation Using Large Language Models

Robert Kunzelmann, Saruni Fernando, Daniela Sanchez Lopera, Jad Al Halabi, Wolfgang Ecker

Super-TCAD: Self-Supervised Graph Attention Networks for Accelerated TCAD Simulations

Tarek Mohamed, Hussam Amrouch

11:00-12:00

Tutorial 2: KAN: Interpretable Machine Learning with Kolmogorov-Arnold Networks

Ziming Liu, MIT

	Moderator: <i>Siddharth Garg, New York University</i>
12:00-13:00	Lunch
13:00-14:00	<p>Session 8: RTL Design with LLM Moderator: <i>Siddharth Garg - New York University</i></p> <p>Rome Was Not Built in a Single Step: Hierarchical Prompting for LLM-based Chip Design <i>Andre Nakkab, Sai Qian Zhang, Ramesh Karri, Siddharth Garg</i></p> <p>Chain-of-Descriptions: Improving Code LLMs for VHDL Code Generation and Summarization <i>Prashanth Vijayaraghavan, Apoorva Nitsure, Charles Mackin, Luyao Shi, Stefano Ambrogio, Arvind Haran, Viresh Paruthi, Ali Elzein, Dan Coops, David Beymer, Tyler Baldwin, Ehsan Degan</i></p> <p>Enhancing the Capabilities of Quantum Transport Simulations Utilizing Machine Learning Strategies <i>Ateeb Naseer, Yawar Hayat Zarkob, Musaib Rafiq, Mohammad Sajid Nazir, Owais Ahmad, Amit Agarwal, Somnath Bhowmick, Yogesh Singh Chauhan</i></p> <p>PyHDL-Eval: An LLM Evaluation Framework for Hardware Design Using Python-Embedded DSLs <i>Christopher Batten, Nathaniel Pinckney, Mingjie Liu, Haoxing Ren, Brucek Khailany</i></p>
14:00-14:15	Break

<p>14:15-15:15</p>	<p>Session 9: Secure Chip Design Moderator: <i>Abdel-Hameed Badawy - New Mexico State University</i></p> <p>An Efficient ML-based Hardware Trojan Localization Framework for RTL Security Analysis (BPA Nominee) <i>Ruchao Fan, Yongming Tang, Hao Sun, Jiyuan Liu, He Li</i></p> <p>Utilizing Reinforcement Learning to Generate Adversarial Hardware Trojan Examples <i>Amin Sarihi, Peter Jamieson, Ahmad Patooghy, Abdel-Hameed Badawy</i></p> <p>LASP: LLM Assisted Security Property Generation for SoC Verification <i>Avinash Ayalasomayajula, Rui Guo, Jingbo Zhou, Sujan Kumar Saha, Farimah Farahmandi</i></p> <p>Automated Physical Design Watermarking Leveraging Graph Neural Networks <i>Ruisi Zhang, Rachel Selina Rajarathnam, David Z. Pan, Farinaz Koushanfar</i></p>
<p>15:15-15:45</p>	<p>Break</p>
<p>15:45-16:45</p>	<p>Session 10: Physical Verification and Testing Moderator: <i>Hao Zheng, University of South Florida</i></p> <p>Parallel Per-tile Activation with Linear Superposition of Thermal Response for Solving Arbitrary Power Pattern in 3DIC Thermal Simulation <i>Haiyang He, Norman Chang, Akhilesh Kumar, Jie Yang, Wenbo Xia, Lang Lin, Jessica Yen, Haoliang Jiang, Rishikesh Ranade</i></p> <p>Efficient and Effective Neural Networks for Automatic Test Pattern Generation <i>Lizi Zhang, Azadeh Davoodi</i></p> <p>LLM Based Physical Verification Runset Generator <i>Luis Francisco, Srinu Arikati</i></p> <p>High-Dimensional Yield Analysis Using Sparse Representation for Long-Tailed Distribution (BPA Nominee) <i>Ziqi Wang, Weihang Sun, Zhongxi Guo, Xiao Shi, Longxing Shi</i></p>
<p>16:45-17:00</p>	<p>Closing Remarks: Hussam Amrouch</p>