MLCAD Program 2024

Sunday, Sept. 8, 2024	
18:30-21:00	**Welcome Reception**
Monday, Sept. 9, 2024	
07:30-08:30	**Breakfast**
08:30-08:45	**Opening Remarks**
08:45-09:30	**Keynote 1:** Jeffrey David, VP of AI Solutions at PDF Solutions **Advancing AI Innovations at Scale for Semiconductor Manufacturing and Test** Moderator: *Hussam Amrouch - Technical University of Munich*
09:30-09:45	**Break**
09:45-10:45	**Session 1: High-Level Synthesis** Moderator: TBD **Learning to Compare Hardware Designs for High-Level Synthesis** *Yunsheng Bai, Atefeh Sohrabizadeh, Zijian Ding, Rongjian Liang, Weikai Li, Ding Wang, Haoxing Ren, Yizhou Sun, Jason Cong* **Cross-Modality Program Representation Learning for Electronic Design Automation with High-Level Synthesis** *Zongyue Qin, Yunsheng Bai, Atefeh Sohrabizadeh, Zijian Ding, Ziniu Hu, Yizhou Sun, Jason Cong* **Automated C/C++ Program Repair for High-Level Synthesis via Large Language Models** *Kangwei Xu, Grace Li Zhang, Xunzhao Yin, Cheng Zhuo, Ulf Schlichtmann, Bing Li* **An ML-aided Approach to Automatically Generate Schematic Symbols in PCB EDA Tools** *Shiyu Gao, Keni Qiu*
10:45-11:15	**Break & Interactive Session**

11:15-12:00	**Session 2: Logic Synthesis** Moderator: *Cunxi Yu, University of Maryland* **ReLS: Retrieval Is Efficient Knowledge Transfer For Logic Synthesis** *Rongjian Liang, Chia-Tung Ho, Anthony Agnesina, Wen-Hao Liu, Haoxing Ren* **Efficient Subgraph Matching Framework for Fast Subcircuit Identification** *Bohao Li, Shizhang Wang, Tinghuan Chen, Qi Sun, Cheng Zhuo* **MinBLoG: Minimization of Boolean Logic Functions using Graph Attention Network (BPA Nominee)** *Prianka Sengupta, Vivek K Rajan, Hesham Mostafa, Somdeb Majumdar, Aakash Tyagi, Jiang Hu*
12:00-13:00	**Lunch**
13:00-14:15	**Special Session 1 (Invited)** Moderator: *Jiang Hu, Texas A&M University* **A3C3 – AI Algorithm & Accelerator Co-design, Co-search, and Co-generation** *Deming Chen, UIUC* **Automating Data Specialization for Machine Learning Acceleration** *Zhiru Zhang, Cornell* **Machine Learning for High Sigma Analog Designs** *Srinivas Jallepalli, NXP Semiconductor*
14:15-14:45	**Break & Interactive Session**

14:45-15:30	**Session 4: Timing Modeling and Analysis** Moderator: *Yibo Lin, Peking University* **FACT: Fast and Accurate Multi-Corner Predictor for Timing Closure in Commercial EDA Flows** *Jiajie Xu, Ziyue Han, Leilei Jin, Shiyang Wu, Hao Yan, LongXing Shi* **Cell Library Characterization for Composite Current Source Models Based on Gaussian Process Regression and Active Learning** *Tao Bai, Zeyuan Deng, Peng Cao* **ML-TIME: ML-driven Timing Analysis of Integrated Circuits in the Presence of Process Variations and Aging Effects** *Xuanyi Tan, Peter Domanski, Sanmitra Banerjee, Krishnendu Chakrabarty*
15:30-16:00	**Break & Interactive Session**
16:00-17:30	**Tutorial 1: Accelerating Semiconductor Industry Innovation with AI/ML: Materials Discovery, Process Optimization, Device Engineering, Chip Design** *Speakers: Gaurav Thareja, Kallol Bera, Ning Zhan, Luca Bracher, Sriram Madhvan - Applied Materials*
17:30-18:00	**Break & Refreshing**
18:00-19:30	**Dinner and Networking**
19:30-21:00	**Panel: ML Enabled CAD – Buy or Develop In-House?** Organizer: *Paul Franzon* Panelists: *Matt Hogan, Siemens* *Mark Ren, NVIDIA* *Thomas Andersen, Synopsys* *Lorenzo Servadei, Sony* *Rajeev Jain, Qualcomm*
Tuesday, Sept. 10, 2024	
07:30-08:30	**Breakfast**

08:30-09:15	**Keynote 2:** *Jinjun Xiong, University at Buffalo*
09:15-09:30	**Break**
09:30-10:30	**Session 5: Physical Design I** Moderator: *Vidya Chhabria - Arizona State University* **Optimizing Predictive AI in Physical Design Flows with Mini Pixel Batch Gradient Descent** *Haoyu Yang, Anthony Agnesina, Haoxing Ren* **Enabling Risk Management of Machine Learning Predictions for FPGA Routability** *Andrew David Gunter, Maya Thomas, Nikhil Pratap Ghanathe, Steven J E Wilton* **Machine Learning VLSI CAD Experiments Should Consider Atomic Data Groups** *Andrew David Gunter, Steven J E Wilton* **OpenROAD-Assistant: An Open-Source Large Language Model for Physical Design Tasks** *Utsav Sharma, Bing-Yue Wu, Sai Rahul Dhanvi Kankipati, Vidya Chhabria, Austin Rovinski*
10:30-11:00	**Break & Interactive Session**
11:00-11:45	**Session 6: Physical Design II** Moderator: TBD **TA3D: Timing-Aware 3D IC Partitioning and Placement by Optimizing the Critical Path** *Donggyu Kim, Minjae Kim, Junseok Hur, Jakang Lee, Jinoh Cho, Seokhyeong Kang* **Flip-flop Centric Incremental Placement for Simultaneous Timing and Clock Network Power Optimization** *Cristhian Roman-Vicharra, Yiran Chen, Jiang Hu* **Human Language to Analog Layout Using Glayout Layout Automation Framework** *Ali Hammoud, Chetanya Goyal, Sakib Pathen, Arlene Dai, Anhang Li, Gregory Kielian, Mehdi Saligane*

11:45-13:00	**Lunch**
13:00-14:30	**Special Session 2 (Invited)** Moderator: *Paul Franzon, North Carolina State University* **Redefining Outliers in Wafer-Based Electrical Testing** *Takashi Sato, Kyoto University* **LLM-Assisted Analytics in Semiconductor Test** *Li-C Wang, UCSB* **Machine Learning in Logic Circuit Diagnosis** *Shawn Blanton, CMU* **When Device Modeling Meets Machine Learning: Opportunities and Challenges** *Lining Zhang, Peking University*
14:30-14:45	**Break**
14:45-15:30	**Session 7: Datasets and Benchmarks** Moderator: *Ulf Schlichtmann, Technical University of Munich* **AutoBench: Automatic Testbench Generation and Evaluation Using LLMs for HDL Design** *Ruidi Qiu, Grace Li Zhang, Rolf Drechsler, Ulf Schlichtmann, Bing Li* **HLSFactory: A Framework Empowering High-Level Synthesis Datasets for Machine Learning and Beyond (BPA Nominee)** *Stefan Abi-Karam, Rishov Sarkar, Allison Seigler, Sean Lowe, Zhigang Wei, Hanqiu Chen, Nanditha Rao, Lizy Kurian John, Aman Arora, Callie Hao* **Thermal Map Dataset for Commercial Multi/Many Core CPU/GPU/TPU** *Jincong Lu, Sheldon Tan*
15:30-16:00	**Break & Interactive Session**
16:00-17:30	**Student Hands-on Workshop by Synopsys** **Organizer:** *Stelios Diamantidis*
17:30-18:30	**Social Event**
18:30-20:30	**Dinner**

Wednesday, Sept. 11, 2024	
07:30-08:30	**Breakfast**
08:30-09:00	**2nd MLCAD Contest Announcement**
09:00-09:45	**Keynote 3:** *Michael Spranger, COO of Sony AI Inc.* **Next-Generation AI for Image Sensing and Entertainment** **Moderator:** *Andrew Kahng, UC San Diego*
09:45-10:15	**Break**
10:15-11:00	**Session 3: Power Grid Analysis and Optimization** Moderator: *Youngsoo Shin - KAIST* **ICDaIR: Distribution-aware Static IR Drop Prediction Flow Based on Image Classification** *Pinquan Li, Yunfan Zuo, Yuwei Sun, Hao Yan, Longxing Shi* **IR-Aware ECO Timing Optimization Using Reinforcement Learning (BPA Nominee)** *Wenjing Jiang, Vidya Chhabria, Sachin Sapatnekar* **A Parallel Simulation Framework Incorporating Machine Learning-Based Hotspot Detection for Accelerated Power Grid Analysis** *Yangfan Jiang, Jianfei Song, Xiaoyu Yang, Xiao Dong, Songyu Sun, Yibo Lin, Zhou Jin, Xunzhao Yin, Cheng Zhuo*
11:00-12:00	**Tutorial 2: KAN: Interpretable Machine Learning with Kolmogorov-Arnold Networks** *Ziming Liu, MIT* Moderator:
12:00-13:00	**Lunch**

13:00-14:00	**Session 8: RTL Design with LLM** Moderator: Siddharth Garg - New York University **Rome Was Not Built in a Single Step: Hierarchical Prompting for LLM-based Chip Design** *Andre Nakkab, Sai Qian Zhang, Ramesh Karri, Siddharth Garg* **Chain-of-Descriptions: Improving Code LLMs for VHDL Code Generation and Summarization** *Prashanth Vijayaraghavan, Apoorva Nitsure, Charles Mackin, Luyao Shi, Stefano Ambrogio, Arvind Haran, Viresh Paruthi, Ali Elzein, Dan Coops, David Beymer, Tyler Baldwin, Ehsan Degan* **Enhancing the Capabilities of Quantum Transport Simulations Utilizing Machine Learning Strategies** *Ateeb Naseer, Yawar Hayat Zarkob, Musaib Rafiq, Mohammad Sajid Nazir, Owais Ahmad, Amit Agarwal, Somnath Bhowmick, Yogesh Singh Chauhan* **PyHDL-Eval: An LLM Evaluation Framework for Hardware Design Using Python-Embedded DSLs** *Christopher Batten, Nathaniel Pinckney, Mingjie Liu, Haoxing Ren, Brucek Khailany*
14:00-14:15	**Break**
14:15-15:15	**Session 9: Secure Chip Design** Moderator: *Hammond Pearce - University of New South Wales Sydney* **An Efficient ML-based Hardware Trojan Localization Framework for RTL Security Analysis (BPA Nominee)** *Ruchao Fan, Yongming Tang, Hao Sun, Jiyuan Liu, He Li* **Utilizing Reinforcement Learning to Generate Adversarial Hardware Trojan Examples** *Amin Sarihi, Peter Jamieson, Ahmad Patooghy, Abdel-Hameed Badawy* **LASP: LLM Assisted Security Property Generation for SoC Verification** *Avinash Ayalasomayajula, Rui Guo, Jingbo Zhou, Sujan Kumar Saha, Farimah Farahmandi* **Automated Physical Design Watermarking Leveraging Graph Neural Networks** *Ruisi Zhang, Rachel Selina Rajarathnam, David Z. Pan, Farinaz Koushanfar*

15:15-15:45	**Break & Interactive Session**
15:45-16:45	**Session 10: Physical Verification and Testing** Moderator: **Parallel Per-tile Activation with Linear Superposition of Thermal Response for Solving Arbitrary Power Pattern in 3DIC Thermal Simulation** *Haiyang He, Norman Chang, Akhilesh Kumar, Jie Yang, Wenbo Xia, Lang Lin, Jessica Yen, Haoliang Jiang, Rishikesh Ranade* **Efficient and Effective Neural Networks for Automatic Test Pattern Generation** *Lizi Zhang, Azadeh Davoodi* **LLM Based Physical Verification Runset Generator** *Luis Francisco, Srini Arikati* **High-Dimensional Yield Analysis Using Sparse Representation for Long-Tailed Distribution (BPA Nominee)** *Ziqi Wang, Weihan Sun, Zhongxi Guo, Xiao Shi, Longxing Shi*
16:45-17:00	**Closing Remarks**: Hussam Amrouch